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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,102	08/14/2001	Oon-Sim Ang	812003	8954

26291 7590 09/09/2005

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EXAMINER	
MERED, HABTE	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

8F

Office Action Summary	Application No.	Applicant(s)	
	09/930,102	ANG ET AL.	
	Examiner	**Art Unit**	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The amendment filed on 21 July 2005 has been entered and fully considered.

2. Claims 1-26 are currently pending.

3. Claim 9 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 9 depends on itself. An art rejection has been provided assuming the Applicant intended dependent claim 9 to depend on independent claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazawa (US 5, 907, 682) in view of Wolf et al (US 6, 526, 069), hereinafter referred to as Wolf.

Miyazawa discloses a device (i.e. shown in Figure 10) that has an overhead processor, frame assembling and disassembling sections, temporary storage devices in the form of registers (See also Figures 14 and 15) for storing different portions of the

overhead part of the frame, and transmit and receive modules. Miyazawa's device is capable of receiving STM-1 transmission frames (structure shown in Figure 1A) from the Network and outputting ATM cells to the ATM layer and vice versa. Even though overhead information processing is not new Miyazawa discloses that his device accomplishes the task with reduced set of hardware ***(See Column 8, Lines 11-47)***

6. Regarding **claims 1, 17 and 20**, Miyazawa discloses a temporary storage device, comprising:

a first buffer, the first buffer configured to receive information, the information provided in association with a line clock signal, the first buffer configured to receive a first write enable signal for storing a first portion of the information; **(The applicant as stated in the specification indicates that a register and any memory can be considered as a temporary device. (See Applicant's Specification, Page 9, Lines 1-4). Given that fact, Miyazawa shows in Figure 10 a device capable of disassembling an STM-1 transmission frame into a payload and overhead component. The entire overhead information is stored in the memory shown as element 3 in Figure 10. (See also column 11, Lines 28-41) Further, Miyazawa discloses, that the overhead information stored is further processed by element 4 in Figure 10, which is referred to as the receiving processor. The receiving processor is further elaborated in Figure 14. Elements 4-6 and 4-7 in Figure 14 or Registers A and B are temporary storage for the overhead information stored earlier in memory. Registers A can be considered as the first buffer and Register B can be considered as the second buffer. Most certainly each register will contain**

different overhead information from one another based on the desired task to be accomplished. (See also column 14, Lines 19-34)

Also, it is clear that the data stored in Registers A and B is associated with the line or network clock signal as there is no system clock provided when storing the data in the registers. The line clock signal must be recovered from the incoming transmission frame to do a write operation in the registers as disclosed by Miyazawa. Of course, recovering line clock signal from the data is known and readily admitted by the applicant and shown as prior art in Figure 1 of the current application being prosecuted.)

a second buffer, the second buffer configured to receive the information, the information provided in association with the line clock signal, the second buffer configured to receive a second write enable signal for storing a second portion of the information different from the first portion of the information; **(Register B in Figure 14 (i.e. 2nd buffer) and see also Column 14, Lines 25-30; Miyazawa meticulously describes in the processing of overhead information how different data is stored in different registers. For instance he shows that H1 and H2 bytes are stored in different registers. See Column 6, Lines 10-15. Miyazawa further shows that the overhead processor 4 of Figure 10 processes the desired data stored in memory 3. See Column 11, Lines 37-41. Miyazawa shows how data in memory 3 is stored intact as an AU pointer, SOH and POH in Column 10, Lines 12-15. The overhead processor 4 of Figure 10 accomplishes the task of choosing which portion of the overhead data to retrieve from memory 3 and where to store it by the use of**

selector 4-5 of Figure 14 as further elaborated in Column 14, Lines 25-29. Further Miyazawa shows the role of the selector in controlling Registers A and B in Column 14, Lines 40-42. Since Miyazawa has already established as part of overhead processing different types of data are stored in different registers and has further shown to have in his system a selector to choose what data to retrieve and store then Registers A and B must be used to store different data.) a pointer processor coupled to the first buffer to receive the first portion of the information, the pointer processor have a third buffer for storing the first portion of the information **(Miyazawa discloses in Figure 11, element 1-10 as a pointer processor in the frame disassembling section and is coupled to Registers A and B of Figure 14 (i.e. 1st and 2nd buffers) and the output of the pointer processor is stored in a third buffer known as status register and shown as element 5 in Figure 10).**

Miyazawa discloses that transmitting and receiving processes can be executed without synchronizing the receive side and transmit side clocks. Miyazawa, however, fails to expressly disclose the use of system clock signal to synchronously clock out data stored in the buffers.

Wolf discloses a synchronization device that receives an input signal a plesiochronic message signal from a PDH system and outputs a synchronous digital message signal (STM-N) into a SDH system. ***(See Column 2, Lines 57-61).*** *Wolf discloses that synchronous operation is accomplished by synchronizing the read clock to the reference clock pulse of the message transmission system. (See column 3, Lines 42-45). Further, Wolf discloses that lowering the write clock from the read clock*

provides an additional advantage in that related VCs (Virtual Containers) will not be outputted with different STM signals ***(See Column 2, Lines 20-27)***.

Wolf discloses a system clock signal provided to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information. **(It would be obvious to apply Wolf's disclosure of using a system clock signal (i.e. a read clock synchronized to a reference clock) to synchronously clock out data from a buffer. See Column 2, Lines 57-61. Wolf applies his disclosure in Figures 3 and 4 where the system clock generator in the CG block is also synchronized with the read clock (RCLK) and also synchronized with the multiplexer (i.e. the unit responsible for creating the STM-N signal) See also Column 4, Lines 15-32 and 55-65)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Miyazawa's apparatus to incorporate the use of system clock signal to synchronously clock out data stored in the buffers and further to keep the write clock lower compared to the read clock, the motivation being to minimize low-frequency phase fluctuations in an inexpensive way and further decrease the likelihood of related VCs in an ATM or digitized video application being sent in different STM-N signal causing integration issue for the far end.

7. Regarding **claim 21**, Miyazawa discloses a temporary storage device further comprising:

a pointer processor coupled to receive the first stored overhead information, the pointer processor have a third buffer for storing the first stored overhead information.

(Miyazawa discloses in Figure 11, element 1-10 as a pointer processor in the frame disassembling section and is coupled to Registers A and B of Figure 14 (i.e. 1st and 2nd buffers) and the output of the pointer processor is stored in a third buffer known as status register and shown as element 5 in Figure 10).

8. Regarding **claims 2 and 22**, Miyazawa discloses a temporary storage device further comprising coupled between the first buffer and the pointer processor, a first reader coupled to receive the first portion of the information from the first buffer and configured to provide a first read enable signal to the first buffer and to provide the first information to the pointer processor. **(Miyazawa discloses in Figure 11, element 1-10 as a pointer processor in the frame disassembling section and is coupled to Registers A of Figure 14 (i.e. 1st buffer). Miyazawa discloses a data is read out of register A. (Miyazawa Column 14, Lines 40-42) There has to be a read enable signal transmitted to read data from any buffer.)**

9. Regarding **claim 3 and 23-25**, Miyazawa discloses a temporary storage device of further comprising:

combinatorial logic configured to provide the first write enable signal, the combinatorial logic configured to provide the first write enable signal in part when selected overhead signals are active**(Miyazawa shows a selector to determine which overhead signals to write in either Register A or Register B. See Miyazawa Column 14, Lines 28-31 and element 4-5 in Miyazawa's Figure 14. The memory access circuit, element 1-3 in Miyazawa's Figure 11, sends a write enable signal to the main buffer where the overhead information is stored. (See Miyazawa Column 13, Lines 1-3). A selector**

has to have some form of combinatorial logic and has to send a write enable signal to Register A or buffer 1 to indicate to it some kind of data is to be written into it);

an overhead extractor-processor **(Element 4 in Miyazawa's Figure 10)** configured to receive the second portion of the information; and

a second reader coupled between the overhead extractor-processor and the second buffer, the second reader coupled to receive the second portion of the information from the second buffer and configured to provide a second read enable signal to the second buffer and to provide the second portion of the information to the overhead extractor-processor.**(The selector in Miyazawa's Figure 14 also acts as the second reader to the second buffer which is Register B. See also Miyazawa's Column 14 Lines 30-35 and 40-42)**

10. Regarding **claim 4**, Miyazawa discloses a temporary storage device wherein the first portion of the information synchronously outputted from the first buffer consists of H1-pointer, H2pointer and H3-pointer information and a synchronous payload envelope. **(The modified invention of Miyazawa and Wolf meets this limitation. When transmitting from the ATM Layer side to the Network, STM signals are created and will have to include H1, H2, and H3 as well as the payload (SPE). Further if the input and output to Miyazawa's device was STM signals then for both transmission and reception H1, H2, and H3 as well as the SPE has to be synchronously outputted using Wolf's technique.)**

11. Regarding **claim 5**, Miyazawa discloses a temporary storage device wherein the second portion of the information synchronously outputted from the second buffer consists of section overhead or line overhead or a combination thereof or consists of regenerator section or multiplex section overhead or a combination thereof.
(Miyazawa indicates the buffers can contain any type of overhead information and is even flexible enough to accommodate future enhancements to the overhead information. See Miyazawa Column 13, Lines 50-54 and Column 8, Lines 15-21)

12. Regarding **claim 6**, Miyazawa discloses a temporary storage device wherein the second write enable signal is a transport overhead signal or a section overhead signal. **(This is strictly a design issue and the applicant has not indicated in a clear manner the merits and advantages of this approach. The applicant's design was addressing sending STM signals in and out of the system and the H1-H3 pointers needed to identify the payload (SPE) were put in buffer 1 which is reasonable and put the remaining overhead info including TOH and SOH in buffer 2. One could have easily interchanged the arrangements in the buffers and be able to send STM signals synchronously either using the applicant system or the modified apparatus of Miyazawa and Wolf. Therefore if the applicant's design is adopted then the 2nd write signal has to be a TOH or SOH).**

13. Regarding **claim 7**, Miyazawa discloses a temporary storage device wherein the second write enable signal is active for providing available columns. **(This is again strictly a design issue and no unique advantage cited by the applicant)**

14. Regarding **claim 8**, Miyazawa discloses a temporary storage device wherein the first portion of the information or the second portion of the information is tagged. **(This is again strictly a design issue and property of SDH/SONET. For instance the headers H1-H3 tag the SPE)**

15. Regarding **claim 9**, Miyazawa discloses a temporary storage device wherein the first portion of the information or the second portion of the information is tagged with an H1-pointer byte. **(This is again strictly a design issue and property of SDH/SONET. For instance the headers H1-H3 tag the SPE)**

16. Regarding **claim 10**, Miyazawa discloses a network node comprising: a receive line interface configured to receive at least one transmission **(See Miyazawa's Figure 10, element 1 input)**;

buffers configured to decouple a line clock signal from input data **(Admitted prior art – see Applicant's Figure 1)**; and

a pointer core **(See Miyazawa's Figure 11, element 1-10)** coupled to receive the first output data from a first buffer of the buffers **(Miyazawa discloses in Figure 11, element 1-10 as a pointer processor in the frame disassembling section and is coupled to Registers A and B of Figure 14 (i.e. 1st and 2nd buffers) and the output of the pointer processor is stored in a third buffer known as status register and shown as element 5 in Figure 10)**, wherein the buffers include:

a first buffer configured to receive a first portion of the input data; and a second buffer configured to receive a second portion of the input data that is different from the first portion <u>**(Miyazawa meticulously describes in the processing of overhead**</u>

information how different data is stored in different registers. For instance he shows that H1 and H2 bytes are stored in different registers. See Column 6, Lines 10-15. Miyazawa further shows that the overhead processor 4 of Figure 10 processes the desired data stored in memory 3. See Column 11, Lines 37-41. Miyazawa shows how data in memory 3 is stored intact as an AU pointer, SOH and POH in Column 10, Lines 12-15. The overhead processor 4 of Figure 10 accomplishes the task of choosing which portion of the overhead data to retrieve from memory 3 and where to store it by the use of selector 4-5 of Figure 14 as further elaborated in Column 14, Lines 25-29. Further Miyazawa shows the role of the selector in controlling Registers A and B in Column 14, Lines 40-42. Since Miyazawa has already established as part of overhead processing different types of data are stored in different registers and has further shown to have in his system a selector to choose what data to retrieve and store then Registers A and B must be used to store different data.)

Miyazawa, however, fails to expressly disclose the use of system clock signal to synchronously clock out data stored in the buffers.

Wolf discloses a system clock signal provided to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information. **(It would be obvious to apply Wolf's disclosure of using a system clock signal (i.e. a read clock synchronized to a reference clock) to synchronously clock out data from a buffer. See Column 2, Lines 57-61. Wolf applies his disclosure in Figures 3 and 4 where the system clock generator in the**

CG block is also synchronized with the read clock (RCLK) and also synchronized with the multiplexer (i.e. the unit responsible for creating the STM-N signal) See also Column 4, Lines 15-32 and 55-65)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Miyazawa's apparatus to incorporate the use of system clock signal to synchronously clock out data stored in the buffers and further to keep the write clock lower compared to the read clock, the motivation being to minimize low-frequency phase fluctuations in an inexpensive way and further decrease the likelihood of related VCs in an ATM or digitized video application being sent in different STM-N signal causing integration issue for the far end.

17. Regarding **claim 11**, Miyazawa discloses a network node further comprising: an overhead extractor-processor coupled to receive the second output data from a second buffer of the buffers (**See Miyazawa's Figure 10, element 4, and Wolf's Figure 3 and 4).**

Miyazawa, however, fails to expressly disclose the use of system clock signal to synchronously clock out data stored in the buffers.

Wolf discloses a system clock signal provided to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information. **(It would be obvious to apply Wolf's disclosure of using a system clock signal (i.e. a read clock synchronized to a reference clock) to synchronously clock out data from a buffer. See Column 2, Lines 57-61. Wolf applies his disclosure in Figures 3 and 4 where the system clock generator in the**

CG block is also synchronized with the read clock (RCLK) and also synchronized with the multiplexer (i.e. the unit responsible for creating the STM-N signal) See also Column 4, Lines 15-32 and 55-65)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Miyazawa's apparatus to incorporate the use of system clock signal to synchronously clock out data stored in the buffers and further to keep the write clock lower compared to the read clock, the motivation being to minimize low-frequency phase fluctuations in an inexpensive way and further decrease the likelihood of related VCs in an ATM or digitized video application being sent in different STM-N signal causing integration issue for the far end.

18. Regarding **claim 12**, Miyazawa discloses a network compromising:

a first multiplexer coupled to receive the first output data from the first buffer and to provide the first output data to the pointer core; **(This is again a design issue. In both the applicant and the references cited some form of multiplexing has to occur to create a main signal from its tributaries)** and

a second multiplexer coupled to receive the second output data from the second buffer and to provide the second output data to the overhead extractor processor. **(This is again a design issue. In both the applicant and the references cited some form of multiplexing has to occur to create a main signal from its tributaries)**

19. Regarding **claim 13**, Miyazawa discloses a network node of wherein the multiplexers are round-robin readers clocked by the system clock signal. **(This is again**

a design issue and applicant has cited no clear advantage of using such approach.)

20. Regarding **claims 14 and 18**, Miyazawa discloses a network node comprising:

a temporary storage device configured to decouple the system clock signal from the data and to couple a line clock signal to the data **(Admitted prior art – see applicant's figure 1)**,

a pointer core having a buffer, the buffer configured to receive the data output from the temporary storage device, the buffer configured to operate on both an input side and an output side synchronous with the line clock signal **(See Miyazawa's Figures 10, 14,15, and 17)**, wherein the buffers include:

a first buffer configured to receive a first portion of the input data; and a second buffer configured to receive a second portion of the input data that is different from the first portion **<u>(Miyazawa meticulously describes in the processing of overhead information how different data is stored in different registers. For instance he shows that H1 and H2 bytes are stored in different registers. See Column 6, Lines 10-15. Miyazawa further shows that the overhead processor 4 of Figure 10 processes the desired data stored in memory 3. See Column 11, Lines 37-41. Miyazawa shows how data in memory 3 is stored intact as an AU pointer, SOH and POH in Column 10, Lines 12-15. The overhead processor 4 of Figure 10 accomplishes the task of choosing which portion of the overhead data to retrieve from memory 3 and where to store it by the use of selector 4-5 of Figure 14 as further elaborated in Column 14, Lines 25-29. Further Miyazawa shows the role</u>**

of the selector in controlling Registers A and B in Column 14, Lines 40-42. Since Miyazawa has already established as part of overhead processing different types of data are stored in different registers and has further shown to have in his system a selector to choose what data to retrieve and store then Registers A and B must be used to store different data.)

Miyazawa, however, fails to expressly disclose the use of system clock signal to synchronously clock out data stored in the buffers. Miyazawa fails to disclose a frame-timing generator, the frame-timing generator configured for synchronous operation off of a system clock signal.

Wolf discloses a frame timing generator, the frame timing generator configured for synchronous operation off of a system clock signal **(See Wolf's Figures 3 and 4 and Column 4, Lines 15-32 and 55-65)** Wolf also discloses a system clock signal provided to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information. **(It would be obvious to apply Wolf's disclosure of using a system clock signal (i.e. a read clock synchronized to a reference clock) to synchronously clock out data from a buffer. See Column 2, Lines 57-61. Wolf applies his disclosure in Figures 3 and 4 where the system clock generator in the CG block is also synchronized with the read clock (RCLK) and also synchronized with the multiplexer (i.e. the unit responsible for creating the STM-N signal) See also Column 4, Lines 15-32 and 55-65)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Miyazawa's apparatus to incorporate the use of system

clock signal to synchronously clock out data stored in the buffers and further to keep the write clock lower compared to the read clock, the motivation being to minimize low-frequency phase fluctuations in an inexpensive way and further decrease the likelihood of related VCs in an ATM or digitized video application being sent in different STM-N signal causing integration issue for the far end.

21. Regarding **claims 15**, Miyazawa discloses a network comprising: a first network node **(See Miyazawa's Figure 10 input to element 1)**; a second network node **(See Miyazawa's Figure 10 output of element 2)**;

a communication link for putting the first network node in communication with the second network node**(Miyazawa's large scale integrated communication shown in Figure 10)**; the first network node configured with a receive buffer, the receive buffer comprising:

a first buffer, the first buffer configured to receive at least a first portion of the overhead information, the at least a first portion of the overhead information provided in association with a line clock signal, the first buffer configured to store a first portion of the at least a first portion of the overhead information; **(Miyazawa Register A in Figure 14 (i.e. 1st buffer) and see also Column 14, Lines 25-30)** and

a second buffer, the second buffer configured to receive at least a second portion of the overhead information, the at least a second portion of the overhead information provided in association with a line clock signal, the second buffer configured to store a second portion of the at least a second portion of the overhead information **(Miyazawa Register B in Figure 14 (i.e. 2nd buffer) and see also Column 14, Lines 25-30)**,

wherein the second portion of the overhead information is different from the first portion of the overhead information **(Miyazawa meticulously describes in the processing of overhead information how different data is stored in different registers. For instance he shows that H1 and H2 bytes are stored in different registers. See Column 6, Lines 10-15. Miyazawa further shows that the overhead processor 4 of Figure 10 processes the desired data stored in memory 3. See Column 11, Lines 37-41. Miyazawa shows how data in memory 3 is stored intact as an AU pointer, SOH and POH in Column 10, Lines 12-15. The overhead processor 4 of Figure 10 accomplishes the task of choosing which portion of the overhead data to retrieve from memory 3 and where to store it by the use of selector 4-5 of Figure 14 as further elaborated in Column 14, Lines 25-29. Further Miyazawa shows the role of the selector in controlling Registers A and B in Column 14, Lines 40-42. Since Miyazawa has already established as part of overhead processing different types of data are stored in different registers and has further shown to have in his system a selector to choose what data to retrieve and store then Registers A and B must be used to store different data.).**

22. Regarding **claim 16 and 19**, Miyazawa discloses a network wherein the receive buffer is located on an input data path in advance of a pointer processor buffer. **(See Miyazawa's Figure 10)**

23. Regarding **claim 26** Miyazawa discloses a temporary storage device of further comprising second combinatorial logic configured to provide a second write enable signal to select the at least a second portion of the overhead information written to the

second buffer. **(Miyazawa shows a selector to determine which overhead signals to write in either Register A or Register B. See Miyazawa Column 14, Lines 28-31 and element 4-5 in Miyazawa's Figure 14. The memory access circuit, element 1-3 in Miyazawa's Figure 11, sends a write enable signal to the main buffer where the overhead information is stored. (See Miyazawa Column 13, Lines 1-3). A selector has to have some form of combinatorial logic and has to send a write enable signal to Register B or buffer 2 to indicate to it some kind of data is to be written into it. It is again a design issue how many combinatorial logic to use.)**

Response to Arguments

24. Applicant's arguments filed 21 July 2005 have been fully considered but they are not persuasive.

25. Applicant in the Remarks, Page 13, argues that in Miyazawa's teaching registers 4-6 and 4-7 are only for holding data selected by selector 4-5 and do not contain different overhead information from one another. Examiner respectfully disagrees with the Applicant's conclusion.

In Miyazawa's teachings there are adequate suggestions leading one having ordinary skill in the art to conclude registers 4-6 and 4-7 contain different overhead information from each another. Miyazawa meticulously describes in the course of processing overhead information how different data is stored in different registers. For instance he shows that H1 and H2 bytes are stored in different registers. See Column 6, Lines 10-15. Miyazawa further shows that the overhead processor 4 of Figure 10 processes the desired data stored in memory 3. See Column 11, Lines 37-41.

Miyazawa shows that data stored in memory 3 is stored intact as an AU pointer, SOH and POH in Column 10, Lines 12-15. The overhead processor 4 of Figure 10 accomplishes the task of choosing which portion of the overhead data to retrieve from memory 3 and where to store it by the use of selector 4-5 of Figure 14 as further elaborated in Column 14, Lines 25-29. Further Miyazawa shows the role of the selector in controlling Registers A and B in Column 14, Lines 40-42. Figures 14and 15 further confirm this in that the selector has ability to choose where it gets data and where it writes its output. Since memory 3 only contains overhead data and is the source to these registers, then only overhead data is stored in these registers.

Since Miyazawa has already established as part of overhead processing different types of data are stored in different registers and has further shown to have in his system a selector to choose what data to retrieve and where to store it then Registers A and B have to be used for storing different overhead data.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to show the state of the art with respect to method and apparatus for transmitting multiple data services simultaneously and synchronously over SONET/SDH:

US Patent (6, 765, 928) to Sethuram et al

US patent (6, 188, 685) to Wolf et al

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HM
08-24-2005

HNguyen

HANH NGUYEN
PRIMARY EXAMINER